# A Novel Parameter-Independent Digital Optimal Control Algorithm for DC-DC Buck Converters Based on Parabolic Curve Fitting


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***Abstract* -- Recently, optimal control on Buck converter for powering the latest computer central processor units (CPUs) has attracted more and more attention. In this paper, a novel digital control algorithm is presented to achieve the time-optimal response for dc-dc Buck converters without relying on any knowledge of converter design parameters such as output inductance, capacitance and even *ESR* value. This algorithm is based on the parabolic curve fitting analysis for deriving the algorithm formulas under the step load transients. Furthermore, this algorithm can be extended to adaptive voltage positioning (AVP) applications with simple modifications for a low *ESR* designed Buck converter. Also, it delivers a practical and cost-effective interface to AVP schemes due to the parameter-independent and current-sensorless detecting mechanism. Finally, simulations and experimental results of a 12 V-1.5 V Buck converter prototype are provided to validate the proposed schemes using digital signal processor (DSP) implementation.**



***Index Terms*—Capacitor Charge Balance Controller, Digital Control, Dc-Dc Buck Converter, Parameter-Independent Algorithm, Optimal Control, Curve Fitting**


## I. INTRODUCTION

The voltage regulation requirements for digital integrated circuits (ICs) power supplies become more stringent under increasing fast load step transient, that is, low output overshoot/undershoot and short settling time. So it becomes more and more difficult to meet the regulation requirements using conventional linear mode controllers such as voltage and current mode controllers of which the design is usually made with the help of small signal model analysis. Normally, due to the undesired voltage deviations, a large volume of output capacitance is required which occupies more board area with linear mode controllers. To break the compensation bandwidth barrier for faster transient response, couples of advanced analog controllers and digital control algorithms have been introduced in some previous literatures without modifying the hardware.

Considerable research has been conducted in "hybrid" (linear/non-linear, *LnL*) type of controllers which are capable of minimizing the voltage deviation and settling time of a dc-dc Buck converter undergoing ultrafast load step transient situation [1]-[12]. Such control methods are often referred to as "optimal control", as well as in this paper. Based on capacitor charge balance control (CBC) concept first introduced in [1], [2], extensive work has been carried out in designing digital CBC controllers that further improves robustness [5]-[8], practical performance [9] and simplicity of the control system [5], [11]. However, all the previous schemes cannot address at least one of the following limitations:

1) Complex real-time calculation is embedded in the algorithm, like division and square root [1]-[4], [12], [13];
2) Current sensing information is required to implement the proposed scheme [1], [2] or its extension for AVP technique [7] [8], adding more cost to the optimal controller and sacrificing the accuracy;
3) Algorithm requires the knowledge of design parameters of passive components mounted in the switched mode power supply [1]-[12];
4) Difficult or impossible to apply AVP technique using the proposed scheme [1], [3], [5];
5) An asynchronous analog to digital converter (ADC) [7] or certain type of active circuitry is required to detect the capacitor current zero-crossover [5], but deteriorating the cost-efficiency, accuracy and robustness of the overall system when the output capacitor has a significant *ESR*;
6) Since only applicable to low *ESR* design [5], [7], the algorithm is *pseudo-parameter independent* and prevented from running for some practical designed converters, for example, with parallel electrolytic output capacitors;

Another observation of the previous techniques is that in order to derive the equations of the proposed optimal algorithms, output capacitor charge and discharge area along with the inductor current is always chosen as a starting or breakthrough point [1]-[12]. But in this paper, a parabolic curve fitting based derivation is shown to provide a possibility for achieving a complete-parameter-independent control strategy (for any reasonable *ESR* value) under load step transients for dc-dc Buck converters. On the other side, AVP scheme is more and more attractive to reduce CPU power dissipation and output capacitance requirement [5], [7], [8]. This proposed algorithm can implement AVP for a low *ESR* Buck converter without adding complexities and computing load to the digital control system. Also, it provides a more suitable interface than some previous time-optimal

AVP schemes without requiring fast current sensing information [5], [7], [8] to detect the load current step value.

The paper is organized as follows. In Section II, the operating principles of the proposed optimal control algorithm for load transients are introduced. Also, in this section, the parameter-independent and current-sensorless mechanism for detecting the critical time points ($t_1$ and $t_2$) for optimal control actions is explained. In Section III, the mathematical expressions of the proposed algorithm are derived based on parabolic curve fitting analysis and extended for AVP applications under modern microprocessor voltage regulators (VRs) design guidelines. The simulations and preliminary experimental results are shown in Section IV to validate the proposed optimal control algorithm, followed by the main conclusions in Section V, finally.

## II. Operating Principles of the Proposed Parameter-Independent Optimal Control Algorithm

### A. Operations of the Proposed Optimal Controller under Load Current Transient Case

Some generally designed Buck converters can carry significant *ESR* in the output capacitor (for example, ceramic capacitors in parallel with OSCON and/or electrolytic capacitors), but all of the existing schemes assume that the *ESR* is negligibly low to derive the algorithms [1]-[12]. But when the *ESR* value is increasing, the algorithm error will rise exponentially to an unacceptable range [1], [3], [4], [7], causing ring-back problem and deteriorating the overall regulation performance and even the stability.

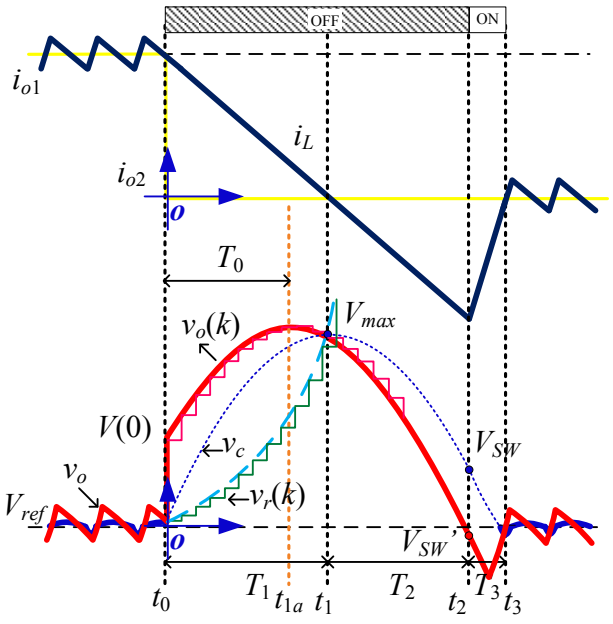


Fig. 1 Inductor current and capacitor voltage waveforms for non-AVP applications ($v_o$: output voltage in red/solid; $v_r$: fitted voltage reference in green/solid; $v_c$: ideal capacitor voltage in dotted line)

For dc-dc Buck converter with significant *ESR*, shown in Fig.1, during negative step load transient, the waveforms of inductor current $i_L$, output voltage $v_o$ and ideal capacitor voltage $v_c$ are illustrated. Mathematically, under the well-established assumption that the inductor current $i_L$ is piecewise linear, the output voltage waveform $v_o$ will present a parabolic shape. If we express the output voltage waveform $v_o$ (in solid red, see Fig. 1) and the ideal capacitor voltage $v_c$ (in dotted blue, see Fig. 1) using the second order time function in the form of (1), they will have exactly the same coefficient $a$ of the quadratic items.

$$v(t) = at^2 + bt + c \tag{1}$$

And this conclusion is always true, even when we consider the parasitic *ESR* and/or *ESL* of the output capacitor. More precisely, in fact, the actual output voltage waveform of the dc-dc buck converter with identical output inductance and capacitance is a family of parabolas which pass the point ($t_1$, $V_{max}$). The mathematical proof is derived in the equations (3)-(10) in the next section.

From the Fig. 1, it is observed that when the capacitor current undergoes zero-crossing at $t_1$, the *ESR* effect on the output voltage will vanish, meaning the voltages $v_o$ and $v_c$ will be identical. So if the shape parameter $a$ has been solved using three known data points, the critical time point $t_1$ can be detected by referring to a fitted curve (2) and comparing with $v_o(t)$. Another crucial time $t_2$, when we set the DPWM signal from low to high, can be determined by using the two-dimensional information; either time ($t$) or output voltage value ($v_o$) based on the function $v_o(t)$.

$$v_r(t) = -at^2 \tag{2}$$

The procedures of the proposed algorithm for negative current step can be briefly listed as follows as an example and applicable for both low and high *ESR* Buck converter designs:

1) Set the DPWM signal to low (for the main switch of the Buck converter), and count the time from the beginning of a current transient happens at $t_0$. Record the initial voltage $V(0)$ after a short period of noise blanking time;

2) Obtain another two sequent voltage samples $v(T)$, $v(2T)$ from ADC at a fixed sampling interval $T$, upon that the ***shape parameter*** $a$ of the parabola curve can be calculated;

3) Build an internal discrete reference voltage signal $v_r(k)$ based on the shape parameter $a$ from the Step 2 and the timing information from Step 1;

4) When the sensed voltage sample $v_o(k)$ (in pink) equals (or smaller than) the reference voltage $v_r(k)$ (in green), $t_1$ will be determined and recorded. Capture the output voltage at $t_1$ (the ideal peak capacitor voltage), referred to as $V_{max}$ in Fig. 1;

5) Calculate the time period $T_2$ or estimate the *switching point voltage* ***(SPV)*** $V_{SW}$ (for capacitor voltage without considering *ESR*) and $V_{SW}'$(for actual output voltage considering *ESR*) as a reference to detect time $t_2$;

6) Set the DPWM to high when $T_2$ ends or the output voltage decreases to SPV $V_{SW}'$ at $t_2$;

7) The conventional PID controller will take back over the regulation task, when the output voltage approaches to the desired value $V_{ref}$ at $t_3$.

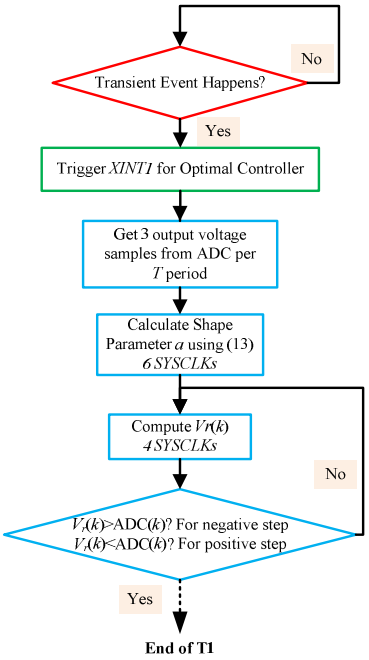


Fig. 2 Program flowchart for determining time $t_1$ using proposed algorithm

The program flowchart of the proposed algorithm for determining time point $t_1$ and the computation information are shown in Fig. 2 using a DSP (TMS320F28027, TI [15]). After the transient happens at $t_0$, the transient detector will trigger the optimal controller to operate for regulation and the ADC will start sampling three output voltage points. By using the proposed algorithm, the parameter $a$ can be solved in only 6 system clock cycles and the discrete reference $V_k(k)$ will be built. The microprocessor will monitor the instant output voltage ADC($k$) and compare it with the reference $V_k(k)$, until $V_k(k)$>ADC($k$) for negative load transient or $V_k(k)$<ADC($k$) for positive load transient.

### *B. Operations of the Proposed Digital Optimal Controller for Active Voltage Positioning*

Since the *ESR*-independent way of determining the time point $t_1$, this proposed method offers a better interface to AVP schemes [8], [9]. And if the converter is designed with low *ESR* output capacitor, for example, using ceramic capacitors, only simple modification is required for implementing AVP based on this algorithm (see Fig. 3). In Step 4, we need to sense the inductor current for estimating the load step $\Delta I$ at $t_1$, and use new formulas (23) and (24) for computing SPV $V_{SW}$. And, finally, the PID controller takes over the regulation task when the output voltage returns to the adaptive voltage position $V_{ref}$-$R_{droop}$·$\Delta I$ instead of $V_{ref}$ (where $R_{droop}$ is the droop resistance). One of the significant benefits of the proposed algorithm for AVP applications is that the load step $\Delta I$ can be estimated based on the parameter $a$ and the output capacitance in equation (25).

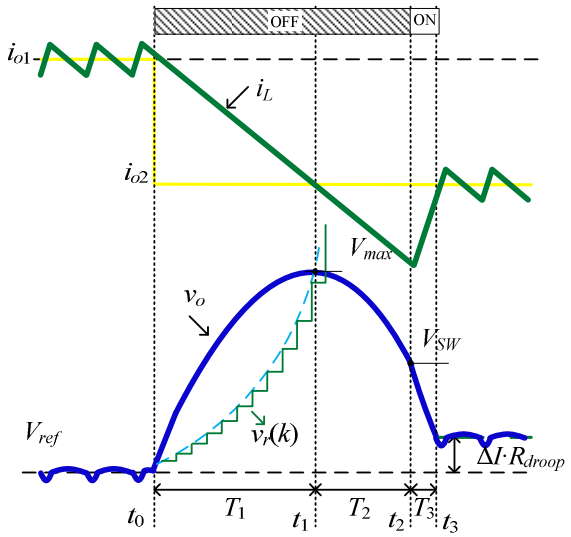


Fig. 3 Inductor current and capacitor voltage waveforms for AVP applications under negative current step change case ($R_{droop}$: droop resistance)

## III. Mathematical Derivations of the Proposed Control Algorithm Based on Parabolic Curve Fitting

In Fig. 1, during the load transients, the waveforms of ideal capacitor voltage and output voltage are illustrated and an imaginary coordinate (in blue) is set up as a reference for the time-based analysis. For negative load step change, during the time period $t_0$-$t_2$ and $t_2$-$t_3$ the capacitor current (ac component of $i_L$) can be approximated as a linear function in (3) and (4), where $m_1$ ($m_1$=$V_{in}$-$V_o$/$L$) and $m_2$ ($m_2$=$V_o$/$L$) are the rising and falling slew rates of the inductor current.

$$i_C(t)\Big|_{t_0\sim t_2} = -m_2(t-t_1) = -\frac{V_o}{L}(t-t_1) \tag{3}$$

$$i_C(t)\Big|_{t_2\sim t_3} = m_1\left(t-t_3+\frac{1}{2}DT_s\right) = \frac{V_{in}-V_o}{L}\left(t-t_3+\frac{1}{2}DT_s\right) \tag{4}$$

As an alternative approach for solving differential equations, the ideal capacitor voltage can be approximated with a parabolic curve in (5) based on the linear output capacitor current in (3) and (4).

$$v_C(t) = -\frac{V_o}{2LC}\left(t^2-2T_1t\right) \tag{5}$$

The output voltage curve can be expressed as (6), where we can discover that even though with a significant *ESR*, the converter output voltage is remaining a *parabolic waveform* and the quadratic coefficient is the same as (5) which is independent on *ESR* value. In the simplified equation (7), the actual output voltage is shifted ahead of a period of time $\Delta t$ with respect to the waveform of the ideal capacitor voltage. And the lead time $\Delta t$ is determined by the product of capacitor value $C$ and its *ESR* value in (8). Even when we consider *ESL* of the output capacitors, it will only affect the constant coefficient of the output voltage polynomial in (9) but not the quadratic coefficient. Because the impact of the *ESL* (-$V_o$/$L$·*ESL* is not more than mV order) is very minor, *ESL* is neglected in the following analysis. When the

capacitor current undergoes a zero crossover, the capacitor voltage $v_C$, reaches its maximum value $V_{\max}$; meanwhile, the output voltage $v_o$ has the same value as $V_{\max}$, which provides an opportunity to attain the information of $t_1$ in (10) (see Fig. 1). Furthermore, another observation can be made that the actual output voltage waveform of the dc-dc buck converter with identical output inductance and capacitance is a family of parabolas which pass the point ($T_1$, $V_{\max}$).

$$v_o(t) = -\frac{V_o}{2LC}\left(t^2 - 2T_1 t\right) + \frac{V_o}{L}(T_1 - t)\cdot ESR \tag{6}$$

$$v_o(t) = -\frac{V_o}{2LC}t^2 + \frac{V_o}{LC}(T_1 - \Delta t)t + \frac{V_o}{L}T_1 \cdot ESR \tag{7}$$

$$\Delta t = T_1 - T_0 = C \cdot ESR \tag{8}$$

$$v_o(t) = -\frac{V_o}{2LC}t^2 + \frac{V_o}{LC}(T_1 - \Delta t)t + \frac{V_o}{L}T_1 \cdot ESR - \frac{V_o}{L}\cdot ESL \tag{9}$$

$$v_o(T_1) = v_c(T_1) = v_r(T_1) = V_{\max} = \frac{V_o}{2LC}T_1^2 \tag{10}$$

To fit the parabolic waveform, three equations are needed for solving the three unknowns in the parabola function in (11), and the variations between the second and first, the third and first output voltage samples are represented as $\Delta v(T)$ and $\Delta v(2T)$. And the simplified equations are shown in (12) and the shape parameter $a$ can be immediately solved using (13). Notice that the equation (13) can be simply calculated by shift operations using DSP in only 6 system clock cycles. Based on this parameter, the internal discrete-time parabolic voltage reference $v_r(k)$ can be built by the formula (14) at the sampling period $T/K$, where $K$ is the constant for resolution adjustment of the reference $v_r(k)$. By comparing $v_r(k)$ with the recent voltage sample $v_o(k)$, time $t_1$ can be detected.

$$\begin{cases} v(0) = c \\ v(T) = aT^2 + bT + c \\ v(2T) = 4aT^2 + 2bT + c \end{cases} \tag{11}$$

$$\begin{cases} \Delta v(T) = v(T) - v(0) = aT^2 + bT \\ \Delta v(2T) = v(2T) - v(0) = 4aT^2 + 2bT \end{cases} \tag{12}$$

$$a = \frac{\Delta v(2T) - 2\Delta v(T)}{2T^2} \tag{13}$$

$$v_r(k) = -\frac{\Delta v(2T) - 2\Delta v(T)}{2T^2}\left(k\frac{T}{K}\right)^2 = -\frac{\Delta v(2T) - 2\Delta v(T)}{2}\left(\frac{k}{K}\right)^2 \tag{14}$$

To determine $t_2$, two methods can be employed and referred to as timing control method and SPV control method in the discussion below.

*Timing control method:* Timing control can be applied, meaning that we exchange the ON/OFF state of the synchronous switches when the calculated time interval $T_2$ (in the equations (15) and (16)) elapses instead of monitoring output voltage and SPV.

$$T_2 = \sqrt{\frac{V_{in} - V_o}{V_{in}}}T_1 = \sqrt{1-D}\,T_1 \tag{15}$$

$$T_2 = \sqrt{\frac{V_o}{V_{in}}}T_1 = \sqrt{D}\,T_1 \tag{16}$$

*SPV control method:* In Fig. 1, alternatively, during the time period $t_1$-$t_2$ and $t_2$-$t_3$, the ideal SPV $V_{SW}$ (without *ESR*) can be calculated using (17) based on the ideal capacitor voltage $v_c$, where the symbol $T_s$ represents the switching period and the $V_{ref}$ is for the output voltage reference, while the equation (18) provides the formula for computing the voltage peak $V_{\max}$. Without sacrificing the accuracy of the algorithm a lot, especially when the switched-mode power supply operates at a very high frequency and narrow duty ratio (12 V-1.5 V), the item $(1/2DT_s)^2$ can be omitted in the equation (17), where $m_1=(V_{in}-V_o)/L$ and $m_2=V_o/L$. Therefore, the formula of voltage $V_{SW}$ can be derived as (19) and simplified in (20). Then, based on the relationship between $T_1$ and $T_2$ in (15) and (16) as well as the initial sampled voltage $V(0)$, the *ESR* included SPV $V_{SW}'$ can be expressed as (21) and (22) for negative and positive current steps, respectively. Notice that all the square root calculations can be done offline or during steady-state.

$$V_{SW} = \frac{1}{2C}m_1\left[T_3^2 - \left(\frac{1}{2}DT_s\right)^2\right] + V_{ref} \tag{17}$$

$$V_{\max} = \frac{1}{2C}m_2T_2^2 + V_{SW} \tag{18}$$

$$V_{SW} = \frac{m_2(V_{\max} - V_{SW})}{m_1} + V_{ref} = \frac{V_o}{V_{in}}V_{\max} + \frac{(V_{in} - V_o)}{V_{in}}V_{ref} \tag{19}$$

$$V_{SW} = DV_{\max} + (1-D)V_{ref} \tag{20}$$

$$V_{SW}' = V_{SW} - V(0)\sqrt{1-D} = DV_{\max} + (1-D)V_{ref} - V(0)\sqrt{1-D} \tag{21}$$

$$V_{SW}' = V_{SW} + V(0)\sqrt{D} = DV_{ref} + (1-D)V_{\min} + V(0)\sqrt{D} \tag{22}$$

In conclusion, according to the derivations discussed above, in the algorithm, neither inductor nor capacitor value is explicit in the final equations (20)-(22). Also, the computation in (20)-(22) is only based on the output voltage information and reference voltage ($V_{ref}$) as well as steady-state duty ratio $D$.

Although both of the methods are very suitable for DSP implementation, SPV control method is more preferred for AVP application. On top of equation (20), similarly, we can compute SPV by simply replacing the voltage reference $V_{ref}$ with ($V_{ref}$-$R_{droop}$·$\Delta I$) for low *ESR* Buck converter in (23) and (24), shown in Fig. 3. Also, using $T_1$ and shape parameter $a$, an estimation can be made for load current step $\Delta I$ in (25) *without requiring current sensing* to realize the AVP technique. This is another significant benefit of the proposed scheme if applied for AVP to optimize the load transient response of a low *ESR* design buck converter.

$$V_{SW} = DV_{\max} + (1-D)\left(V_{ref} - R_{droop}\cdot\Delta I\right) \tag{23}$$

$$V_{SW} = D\left(V_{ref} - R_{droop}\cdot\Delta I\right) + (1-D)V_{\min} \tag{24}$$

$$\Delta I = -\frac{V_0}{L}T_1 = 2aCT_1 \tag{25}$$

## IV. Validation of the Proposed Optimal Response Algorithm

### A. Simulation Results

In order to verify the functionalities of the proposed optimal algorithm, a Buck converter model undergoing different transient conditions is simulated. And the simulated results are shown in the Figures 4-7. The simulation model parameters are listed as follows: $V_{in}$=12 V, $V_o$=$V_{ref}$=1.5 V, $f_s$=350 *k*Hz, $L$=1 $\mu$H, $R_L$=1 $m\Omega$, $C$=180 $\mu$F, $ESL$=100 $p$H. And the *ESR* of the output capacitor is chosen to be 0.5 $m\Omega$ for low *ESR* design and 30 $m\Omega$ for significant *ESR* simulations.

In Fig. 4 and Fig. 5, the transient response performance of the aforementioned dc-dc buck converter model using proposed digital optimal controller is shown. For positive step load transient, if the converter has low *ESR* value, the voltage undershoot is much smaller than that with large *ESR*, but the settling time is quite similar. In addition, under negative load transient, the voltage overshoot is higher for large *ESR* converter because of the voltage contributed from the *ESR* and the large load step change. Also, the difference of the settling time between low and high *ESR* buck converter is minor.

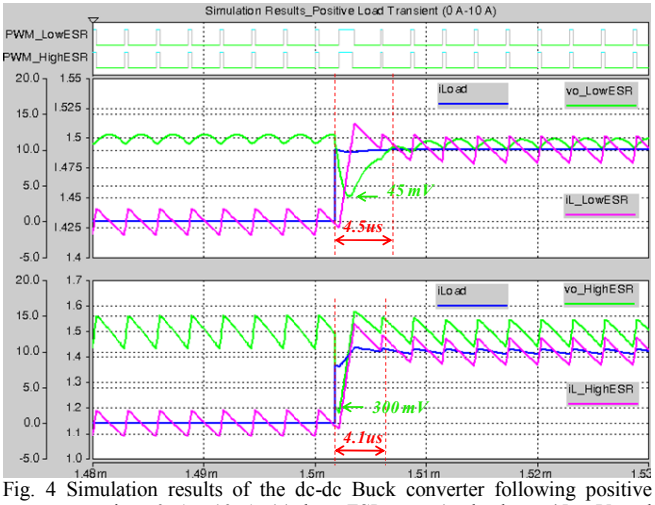


Fig. 4 Simulation results of the dc-dc Buck converter following positive current transient 0 A→10 A (a) low *ESR* case (undershoot 45 mV and settling time 4.5 µs); (b) large *ESR* case (undershoot 300 mV and settling time 4.1 µs) using proposed optimal controller;

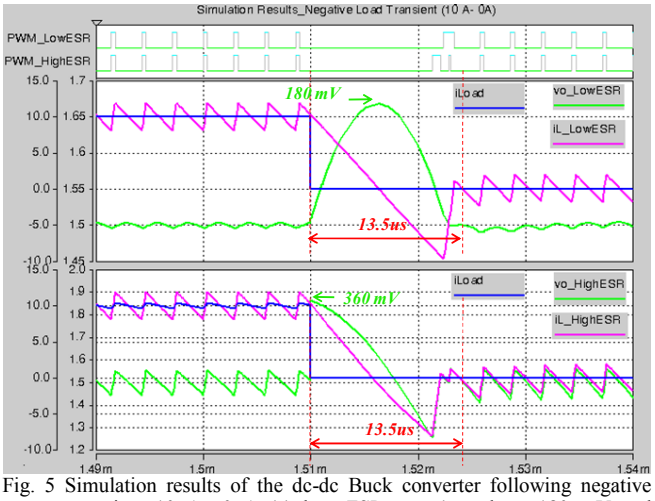


Fig. 5 Simulation results of the dc-dc Buck converter following negative current transient 10 A→0 A (a) low *ESR* case (overshoot 180 mV and settling time 13.5 µs); (b) large *ESR* case (undershoot 360 mV and settling time 13.5 µs) using proposed optimal controller;

In Fig. 4 and Fig. 5, the top section shows the DPWM signal for both of the cases. And the load current (iLoad), output voltage (vo) and inductor current waveforms (iL) are shown in the two sections on the bottom.

Also for comparison purposes, a well-design PID controller (bandwidth: ≈75 *k*Hz, Phase margin ≈60 °) is also simulated for regulating the dc-dc buck with low *ESR* as shown in Fig. 6 and Fig. 7. The PWM signals are shown for the comparison between proposed optimal controller (sw_CBC) and linear voltage mode controller (sw). The inductor current (iL) and output voltage waveforms (vo) are also simulated with two types of controllers.

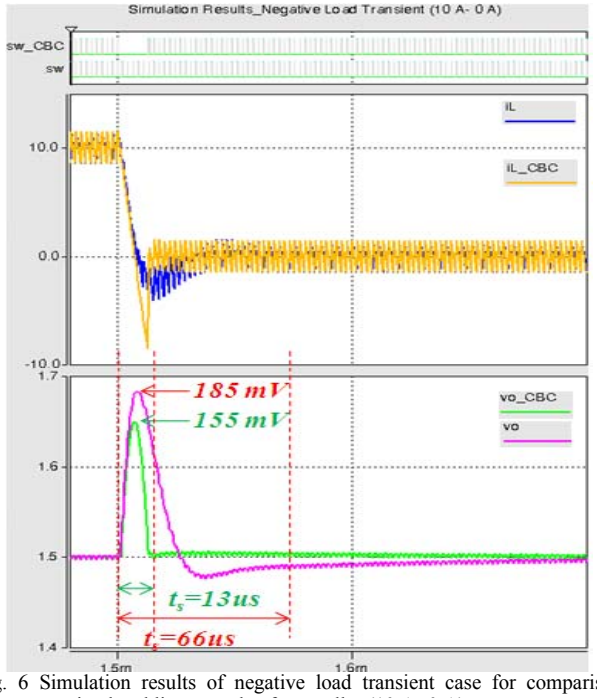


Fig. 6 Simulation results of negative load transient case for comparison between optimal and linear mode of controller (10 A -0 A)

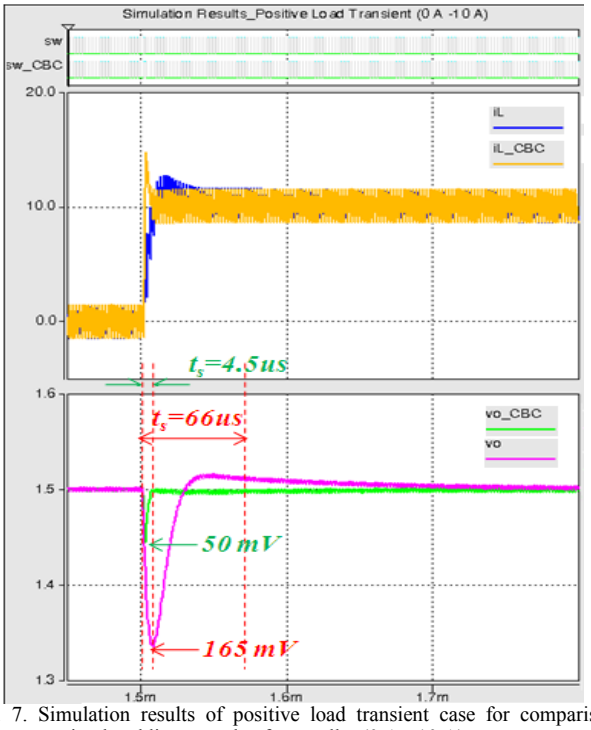


Fig. 7. Simulation results of positive load transient case for comparison between optimal and linear mode of controller (0 A - 10 A)

To sum up, under the load transient cases, for negative step, the overshoot is reduced by 16% and settling time is shortened by 80%, while for positive step, the voltage undershoot is reduced by 70% and settling time is shortened by 93%.

*B. Design Prototype and Experimental Results*

A prototype is designed using the parameters in the simulations with different output capacitors. Because the proposed scheme is very suitable for DSP implementation by using its external interrupts and peripherals, such as timer, ePWM, ADC and digital comparator, a fixed-point 32-bit DSP TMS320F28027 is employed to implement the proposed digital optimal control algorithm, which is shown in Fig. 8.

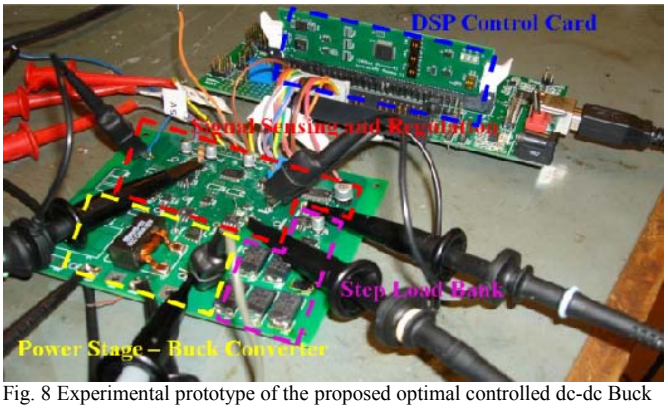


Fig. 8 Experimental prototype of the proposed optimal controlled dc-dc Buck converter

Experimental results, shown in Fig. 9 and Fig. 10, demonstrate the transient performance of conventional linear voltage mode controller (bandwidth: ≈75 *k*Hz, Phase margin ≈60 °) under the load current step change between no load (0 A) and full load (10 A). Limited by the compensation bandwidth, the linear voltage mode controller will cause larger voltage variations and recovery time than optimal controller. For positive load transient, the voltage undershoot is about 170 mV with 61 $\mu$s settling time, while, the overshoot is about 185 mV with 56 $\mu$s settling time. Notice that the difference between the simulation results in Fig. 6, 7 and experimental results in Fig.9, 10 is caused by the different step load transient timing.

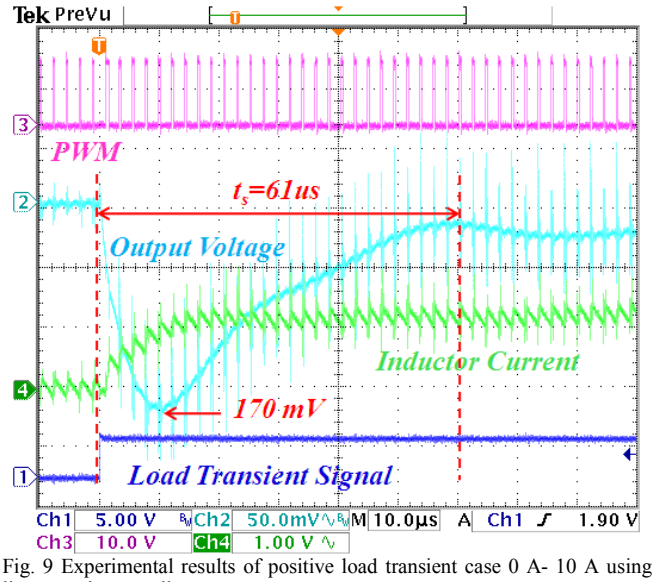


Fig. 9 Experimental results of positive load transient case 0 A- 10 A using linear mode controller

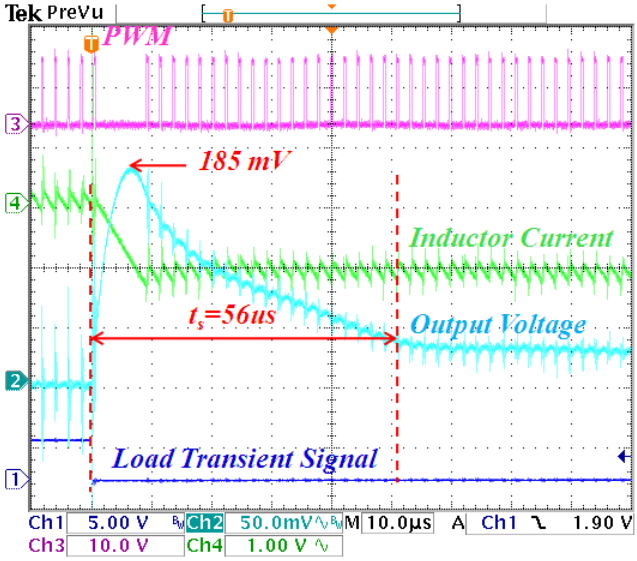


Fig. 10 Experimental results of negative load transient case 10 A- 0 A using linear mode controller

Experimental results of the proposed optimal controller are shown in Figures 11-14, under the load step change between no load (0 A) and full load (10 A). And in order to

demonstrate the applicability of the proposed scheme for any reasonable *ESR* value, paralleled ceramic capacitors (*ESR*≈0.5 *m*Ω, see Fig. 11 and 12) and aluminum electrolytic capacitors (*ESR*≈30 *m*Ω, see Fig. 13 and 14) are employed for output capacitance around 180 $\mu$F. In the experiments, the aforementioned timing control method is used, because of the unified form for low or large *ESR* cases. The proposed controller demonstrates quite similar improved performance as its analog counterpart [3] and even maintains a good settling performance for significant *ESR* case.

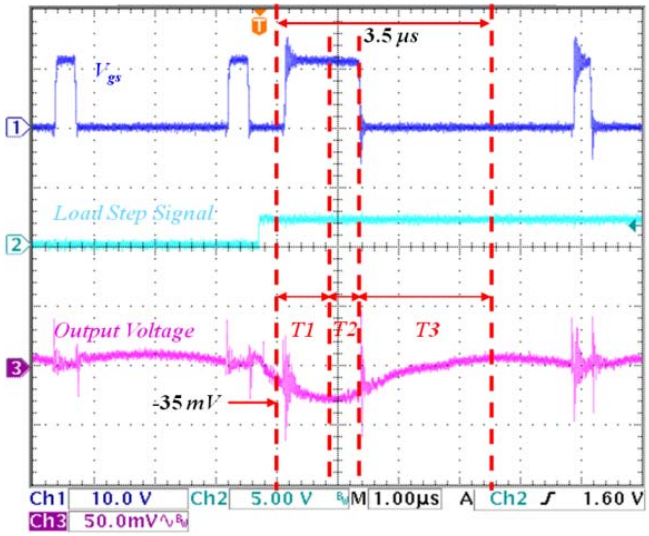


Fig. 11 Experimental results of positive load transient case 0 A- 10 A using optimal controller for low *ESR* buck converter

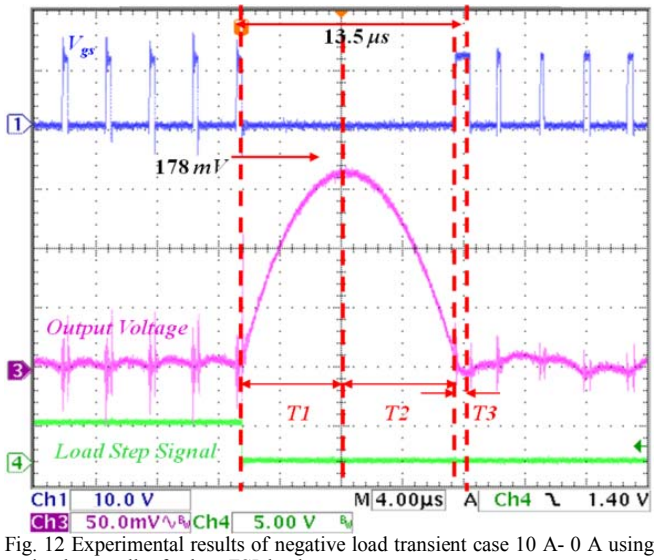


Fig. 12 Experimental results of negative load transient case 10 A- 0 A using optimal controller for low *ESR* buck converter

For low *ESR* cases, compared with the well-designed voltage mode PID controller (see Fig. 9 and 10), under a 10 A positive load step transient, the settling time is improved by 94 % and the voltage undershoot is reduced by 79 %. For a 10 A negative load step change, although the voltage overshoot is not improved because of the narrow operating duty ratio, the settling time is still shortened by 82 % using proposed time-optimal controller.

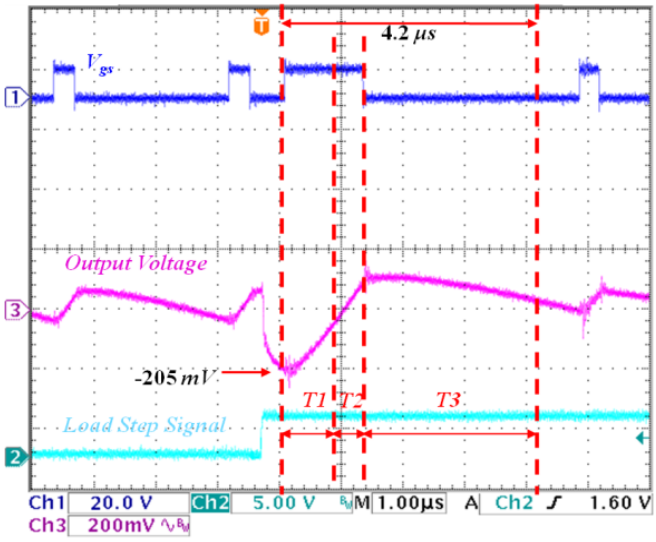


Fig. 13 Experimental results of positive load transient case 0 A- 10 A using optimal controller for large *ESR* buck converter

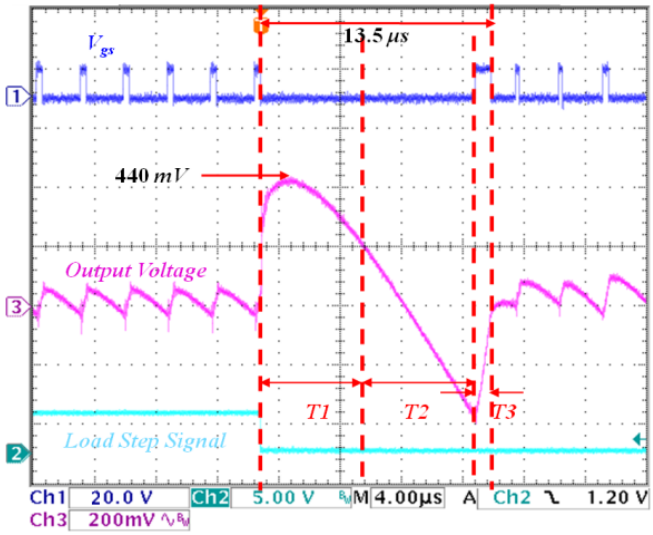


Fig. 14 Experimental results of negative load transient case 10 A- 0 A using optimal controller for large *ESR* buck converter

In order to verify the applicability of the proposed scheme for any reasonable *ESR* value, paralleled electrolytic capacitors (*C*=180 $\mu$F, *ESR*=30 *m*Ω) are employed as the output capacitor (see Fig. 13 and 14). The experimental results are shown in Fig. 13 and Fig. 14, as discussed in the previous sections, although the voltage deviation is larger than that of the low *ESR* case, the settling time is quite similar. For positive step load transient case, the voltage undershoot is 205 mV with 4.2 $\mu$s settling time. And for negative load step change, the voltage overshoot is about 440 mV and the settling time is 13.5 $\mu$s.

## V. CONCLUSIONS

In this paper, a parabolic curve fitting method is employed to design the proposed time-optimal controller. It is demonstrated through simulations and experimental results, that the proposed parameter-independent algorithm can be implemented for any practical designed Buck converter to optimize the transient performance. Further, the proposed controller demonstrates quite similar improved performance as its analog counterpart and even maintains a good performance for significant *ESR* case. Also a promising possibility is shown for AVP technique using this scheme for powering modern microprocessors with load current step estimation.

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